Docket No.: 50006-073

UTILITY PATENT APPLICATION
UNDER 37 CFR 1.53(b)

Box PATENT APPLICATION
Assistant Commissioner for Patents
Washington, DC 20231
Sir:

Transmitted herewith for filing is the patent application of:

INVENTOR: Isao NOJIRI, Ryu MAKABE
FOR: SEMICONDUCTOR DEVICE AND ITS WIRING METHOD

Enclosed are:

- ☒ 28 pages of specification, claims, abstract.
- ☒ Declaration and Power of Attorney.
- ☒ Priority Claimed.
- ☒ Certified copy of Japanese Patent Application No. 2000-007923
- ☒ 10 sheets of formal drawing.
- ☒ An assignment of the invention to Mitsubishi Denki Kabushiki Kaisha and the assignment recordation fee.
- ☐ An associate power of attorney.
- ☐ A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27.
- ☒ Information Disclosure Statement, Form PTO-1449 and reference.
- ☒ Return Receipt Postcard
- ☒ Preliminary Amendment

The filing fee has been calculated as shown below:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	AMOUNT
Total Claims	9	-20	0	$18.00	$0.00
Independent Claims	3	-3	0	$78.00	$0.00
				Multiple Dependent Claim(s)	$0.00
				Basic Fee	$690.00
				Total of Above Calculations	$690.00
				Less ½ for Small Entity	$0.00
				Assignment & Recording Fee	$40.00
				Total Fee	$730.00

☒ Please charge my Deposit Account No. 500417 in the amount of $730.00. A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 500417. A duplicate copy is enclosed.

- ☒ Any additional filing fees required under 37 CFR 1.16.

☒ The Commissioner is hereby authorized to charge payment of the following fees during the pendency of this application or credit any overpayment to Deposit Account No. 500417. A duplicate copy of this sheet is enclosed.

- ☒ Any patent application processing fees under 37 CFR 1.17.
- ☒ Any filing fees under 37 CFR 1.16 for presentation of extra claims.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Stephen A. Becker
Registration No. 26,527

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 SAB:klm
Date: September 5, 2000
Facsimile: (202) 756-8087

Docket No.: 50006-073 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	
	:	
Isao NOJIRI, et al.	:	
	:	
Serial No.:	:	Group Art Unit:
	:	
Filed: September 05, 2000	:	Examiner:
	:	

For: SEMICONDUCTOR DEVICE AND ITS WIRING METHOD

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

Prior to examination of the above-referenced application, please amend the application as follows:

IN THE CLAIMS:

Claim 5, line 1, please change "claim 5" to --claim 4--.

Claim 8, line 1, please change "claim 8" to --claim 7--.

REMARKS

Entry of this preliminary amendment is respectfully requested.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Stephen A. Becker
Registration No. 26,527

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 SAB:klm

Date: September 5, 2000

Facsimile: (202) 756-8087

SEMICONDUCTOR DEVICE AND ITS WIRING METHOD

FIELD OF THE INVENTION

The present invention relates to a semiconductor device to be mounted on a mother board and a wiring method for the semiconductor device. In particular, the present invention relates to a semiconductor device such as chipset which includes a circuit board (daughter board) and one or more chips each incorporating one or more semiconductor elements, wherein a connection pad on the chip is electrically connected with another connection pad on the circuit board through a bonding wire, for example. Also, the present invention relates to a method for wiring the semiconductor device or chipset.

BACKGROUND OF THE INVENTION

In order to mount semiconductor devices or components such as chipsets as many as possible on a limited area of a mother board, a variety of stacked-chip package such as S-CSP (Stacked Chip Scale Package) and S-MCP (Multi Chip Package) have been provided in the art. Typically, the package includes a daughter board to be positioned on the mother board and one or stacked plural semiconductor chips mounted on either or both surfaces of the daughter board.

Figs. 11 and 12 illustrate an example of the conventional stacked package (S-CSP) generally indicated by reference numeral 100. The package 100 includes a daughter board in the form of circuit board 102. The circuit board 102 is wired on its top surface with an electric circuit including a plurality of connection pads or bonding pads 104(104_1-104_5) and is provided on its bottom surface with a number of solder balls 106 corresponding to the bonding pads 104, so that each pair of bonding pad 104 and solder ball 106 is electrically connected through a corresponding through-hole 108 formed in the circuit board 102. The circuit board 102 bears first and second semiconductor chips 110 and 112 manufactured through a well-known semiconductor manufacturing process and stacked in this order on the top surface of the circuit board 102. The first semiconductor chip 110 has bonding pads 114 (114_2, 114_4) electrically connected with circuit elements formed in the chip. The second semiconductor chip 112 on the other hand includes another bonding pads 114 (114_1, 114_3, 114_5) electrically connected with electric elements formed in the chip. The bonding pads of the first and second semiconductor chips 110 and 112 are arranged so that, when viewed from the Y-Y' direction, the bonding pad 114_2 positions between the bonding pads 114_1 and 114_3 and the bonding pad 114_4 positions between the bonding pads 114_3

and 114_5. Also, the bonding pads 114_1-114_5 are electrically connected with the corresponding bonding pads 104 (104_1-104_5) mounted on the circuit board 102 through respective gold bonding wires. Then, the circuit board 102 with the first and second semiconductor chips 110 and 112 so constructed is sealed by a suitable resin so that the resin covers the chips 110 and 112 and boding wires 116. Thereby, the semiconductor device is completed. It should be noted that the commercially available semiconductor device includes more bonding pads on the circuit board and/or the first and second semiconductor chips; however, only a part of which is illustrated in Figs. 10 and 11 for the clarification of those drawings.

The above-described semiconductor device 100 in which the semiconductor chips 110 and 112 are electrically connected with the circuit board 102 through bonding pads 104 and 114 mounted thereon and bonding wires 116 extending between corresponding bonding pads requires the bonding pads 114_1-114_5 of the semiconductor chips 110 and 112 and bonding pads 104_1-104_5 of the circuit board 102 to be arranged in this order in the X-X' direction, respectively. Specifically, as shown in Fig. 12, the five bonding pads 104_1-104_5 aligned in the X-X' direction on the circuit board 102 should be related with the bonding pads 114_1-114_5 on the semiconductor chips 110 and 112. This is because

that, when assuming that the bonding pad 104_5 on the circuit board 102 is connected with another bonding pad 114_1 on the semiconductor chip 112, positioned on the opposite side with respect to the X-X' direction, through the bonding wire 116, the bonding wire would crosse and then make short circuits with another bonding wires.

However, in order to make an electrical connection between the circuit on the mother board and the electric component positioned on the mother board, a practical requirement still exists in which, for example, the bonding pad 114_1 on the semiconductor chip 112 is connected with the bonding pad 104_5 on the circuit board 102. This can be attained by changing the circuit pattern in the semiconductor chips 110 and 12 according to the circuit patterns of the mother boards, which disadvantageously requires a variety of exposure masks for the circuits of the chips.

SUMMARY OF THE INVENTION

Therefore, an object of the present invention is to provide a semiconductor device and its wiring method which allow the connection pads on the semiconductor chips to be connected with corresponding electrical connecting portions on the circuit board or daughter board, which would not subject to the restrictions imposed by the wire

bonding.

Another object of the present invention is to provide a semiconductor device capable of being mounted on a variety of mother boards without any need to change the circuit pattern of the semiconductor chips

Another object of the present invention is to provide a semiconductor device which allows the circuit board to be electrically connected with the semiconductor chips mounted on the board beyond a range in which the wire bonding can apply.

Accordingly, a semiconductor device mounted on a mother board comprises a circuit board to be positioned on the mother board, and a semiconductor chip positioned on the circuit board. The circuit board has a connection pad, a relay pad spaced away from the connection pad, and a wire connecting between the connection pad and the relay pad on a surface of the circuit board supporting the semiconductor chip. Also, the semiconductor chip has a connection pad corresponding to the connection pad formed on the circuit board. Further, the connection pad on the circuit board and the connection pad on the semiconductor chip are electrically connected through a bonding wire.

The wire connecting between the connection pad and the relay pad on the circuit board may be printed on the circuit board with the connection pad and the relay pad.

Also, the wire connecting between the connection pad and the relay pad on the circuit board may be a bonding wire.

Another semiconductor device comprises a first semiconductor chip having a connection pad, a second semiconductor chip positioned on the first semiconductor chip, the second semiconductor chip having a connection pad, wherein the electrode on the second semiconductor chip is electrically connected with the connection pad on the first semiconductor chip.

The connection pad on the first semiconductor chip may be connected with the connection pad on the second semiconductor chip through a bonding wire.

Also, the connection pad on the first semiconductor chip positions in a region where the first semiconductor faces to the second semiconductor chip, the connection pad on the second semiconductor chip in the region, and the connection pad on the first semiconductor chip is electrically connected with the connection pad on the second semiconductor chip through a conductive member positioned in the region.

Another wiring method comprises the steps of:

providing a first semiconductor chip having a connection pad;

positioning a second semiconductor chip on the

first semiconductor chip, the second semiconductor chip having a connection pad; and

electrically connecting between the connection pad of the first semiconductor chip and the connection pad of the second semiconductor chip.

The connection pad of the first semiconductor chip may be electrically connected with the connection pad of the second electrode through a bonding wire.

Also, the connection pad on the first semiconductor chip positions in a region where the first semiconductor faces to the second semiconductor chip and the connection pad on the second semiconductor chip positions in the region, and the connection pad on the first semiconductor chip is electrically connected with the connection pad on the second semiconductor chip through a conductive member positioned in the region.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a partial perspective view of a semiconductor device according to the first embodiment of the present invention;

Fig. 2 is side elevational view of the semiconductor device in Fig. 1;

Fig. 3 is a partial perspective view of a semiconductor device according to the second embodiment of

the present invention;

Fig. 4 is a partial perspective view of a semiconductor device according to the third embodiment of the present invention;

Fig. 5 is a partial perspective view of a semiconductor device according to the fourth embodiment of the present invention;

Fig. 6 is a partial perspective view of a semiconductor device according to the fifth embodiment of the present invention;

Fig. 7 is a partial perspective view of a semiconductor device according to the sixth embodiment of the present invention;

Fig. 8 is a partial perspective view of a semiconductor device according to the seventh embodiment of the present invention;

Fig. 9 is a partial perspective view of a semiconductor device according to the eighth embodiment of the present invention;

Fig. 10 is a partial perspective view of a semiconductor device according to the ninth embodiment of the present invention;

Fig. 11 is a side elevational view of a stacked chip package (S-CSP) of a conventional semiconductor; and

Fig. 12 is a pespective view of the stacked chip

package in Fig. 11.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

With reference to the drawings, descriptions will be made to various preferred embodiments of the present invention. Note that in the following discussions like reference numerals designate like parts or portions throughout the drawings.

EMBODIMENT 1

Figs. 1 and 2 illustrate respective parts of a semiconductor device of the first embodiment. The semiconductor device, generally indicated by reference numeral 10, is a semiconductor electric component such as arithmetic and memory devices to be mounted on a substrate or mother board 12 together with similar semiconductor devices and other electric components. The semiconductor device 10 includes a circuit board 14. Typically, the circuit board 14 employs a rectangular board (daughter board) bearing certain circuits printed on its opposite surfaces. Also, the board is made of suitable insulator such as polyimide or the mixture of glass and epoxy resin.

The circuit printed on the top surface of the circuit board 14 has a plurality of connection pad or bonding pads 16_{X1}, 16_{X2}, ..., $16_{Y1}'$, 16_{Y2}, 16_{Y3},... along and

beside one edge of the circuit board, extending in the X-X' and Y-Y' directions perpendicular to each other. Also, the board 14 bears a connection pad 18 spaced a certain distance away from the pad 16_{Y1}' (referred to as "relay pad" as necessary) in the Y-Y' direction and a connecting wire 20 printed on the board for the electrical connection between the relay pad 16_{Y1}' and the connection pad 18. As shown in Fig. 2, the bottom surface of the circuit board 14 holds a plurality of solder balls 22 for the corresponding bonding pads 16_{X1}, 16_{X2}, ..., 16_{Y2}, 16_{Y3}, ...and connection pad 18 except for the relay pad 16_{X1}'. Also, the solder balls 22 are electrically connected with the corresponding bonding pads 16_{X1}, 16_{X2}, ..., 16_{Y2}, 16_{Y3}, ...and connection pad 18 through, for example, respective through-holes 24 (see Fig. 2) extending between the top and bottom surfaces of the circuit board 14.

The circuit board 14 supports the first semiconductor chip 26 on its top surface. The first semiconductor chip 26 is designed to be smaller than the circuit board 14 so that a marginal portion of the circuit board 14 supporting the electrodes exposes to air around the semiconductor chip 26 as shown in Fig. 1. The first semiconductor chip 26 in turn supports the second semiconductor chip 30 on its top surface. The second semiconductor chip 30 is designed to be smaller than the

first semiconductor chip 26 so that a marginal portion of the first semiconductor chip 26 exposes to air around the second semiconductor chip 30. The first and second semiconductor chips 26 and 30 may be secured on the circuit board 14 and the first semiconductor chip 26, respectively, by means of a suitable bonding material. Although not only the circuit board 14 but also the first and second semiconductor chips 26 and 30 have rectangular plane configurations, they may have another plane configurations.

The first and second semiconductor chips 26 and 30 each have one or more semiconductor elements such as transistor formed through the semiconductor manufacturing process including several steps such as film formation, etching, and exposure. In particular, the first semiconductor chip 26 bears connection pads or bonding pads 32_{X1}, 32_{Y2}, ... along edges extending in the X-X' and Y-Y' directions. Likewise, the second semiconductor chip 30 bears bonding pads 32_{X2}, 32_{Y1}, 32_{Y2}, ... along edges extending in the X-X' and Y-Y' directions. The bonding pads 32_{X1}, 32_{X2}, ..., 32_{Y1}, 32_{Y2}, 32_{Y3}, ... are located corresponding to the bonding pads 16_{X1}, 16_{X2}, ..., $16_{Y1}'$, 16_{Y2}, 16_{Y3}, ... on the circuit board 14. Specifically, for the bonding pads arranged along and beside the edges extending in the Y-Y' direction, the corresponding bonding pads $16_{Y1}'$ and 32_{Y1}, 16_{Y2} and 32_{Y2}, and 16_{Y3} and 32_{Y3} are positioned on

respective lines extending in the X-X' direction. Likewise, for the bonding pads arranged along and beside the edges extending in the X-X' direction, the corresponding bonding pads 16_{X1} and 32_{X1}, 16_{X2} and 32_{X2}, and 16_{X3} and 32_{X3} are positioned on respective lines extending in the Y-Y' direction.

It should be noted that the bonding pads 32_{X1}, 32_{X2}, ..., 32_{Y1}, 32_{Y2}, 32_{Y3}, ... may be formed in the process of the semiconductor manufacturing process or may be formed in another process by the use of a well known printing technique, for example. Also, after the first and second semiconductor chips 26 and 30 has been secured on the circuit board 14, the bonding pads 32_{X1}, 32_{X2}, ..., 32_{Y1}, 32_{Y2}, 32_{Y3}, ... are electrically connected with corresponding bonding pads 16_{X1}, 16_{X2}, ..., $16_{Y1}'$, 16_{Y2}, 16_{Y3}, ... by extending the bonding wires of gold therebetween. Finally, although not shown, the semiconductor chips 26 and 30, including bonding wires 34 and bonding pads, are covered with a suitable sealant made of insulator.

The semiconductor device 10 so constructed is positioned on the mother board 12 which is generally far greater than the circuit board 14 and then heated in a suitable furnace (not shown) such as reflow furnace for melting the solder balls. This causes the semiconductor chips 26 and 30 to be secured and connected permanently

with the circuit of the mother board. Therefore, even though the bonding pad 32_{X1} is offset from the bonding pad 32_{Y1} in the Y-Y' direction when the semiconductor chips 26 and 30 have been mounted on the circuit board 14, it is electrically connected with the associated portion of the circuit board 14 or connection pad 18 through the bonding pad or relay pad 16_{Y1}'. This means that, simply by using the relay pad on the circuit board 14 and without changing the circuit design (i.e., mask pattern) of the semiconductor chip 30, the bonding pads of the semiconductor chips 26 and 30 are suitably connected with the corresponding circuit portions on the mother board. Accordingly, with the semiconductor device 10, no physical contacts or interference with another bonding wires which has been described above will be formed.

SECOND EMBODIMENT

Fig. 3 illustrates a part of the semiconductor device, generally indicated by reference numeral 10_2, according to the second embodiment of the present invention. In the semiconductor device 10_2, the circuit formed on the circuit board 14 includes a connecting bonding pad 16_{Y0} spaced a certain distance away from the relay pad 16_{Y1}' in the Y-Y' direction. The first semiconductor chip 26 bears relay pads 32_{Y1}' and 32_{Y0}' spaced away from each other in

the Y-Y' direction and a connecting wire 36 extending between the relay pads 32_{Y1}' and 32_{Y0}' for the electrical connection of the electrodes. The circuit board 14 supports a solder ball (not shown) on the bottom surface of the board so that the solder ball opposes the bonding pad 16_{Y0}. The solder ball and the opposing bonding pad 16_{Y0} are electrically connected through a through-hole (not shown). Bonding wires 34 are extended between the connecting bonding pad 16_{Y0} and the relay pad 32_{Y0}', relay pads 32_{Y1}' and 16_{Y1}', and the relay pad $16Y_1$' and the bonding pad 32_{Y1} of the second semiconductor chip 30. This causes an electrical connection between the bonding pad 32_{Y1} and the connecting bonding pad 16_{Y0} shifted from the bonding pad 32_{Y1} in the Y-Y' direction.

With the semiconductor device 10_2, similar to the first embodiment, the bonding pads of the semiconductor chips 26 and 30 can properly be connected with the corresponding circuit portions on the mother board by providing minor changes to the mask patterns of the semiconductor chip 26 and the circuit board without providing any design change to the circuit or relay pads on the circuit board 14. Also, even where no space remains for the wire 20 on the circuit board 14 as shown in Fig. 1, the physical contact or interference of the bonding wires will be eliminated by the transit wire on the semiconductor

chip.

THIRD EMBODIMENT

Fig. 4 illustrates a part of the semiconductor device, generally indicated by reference numeral 10_3, according to the third embodiment of the present invention, which is a modification of the second embodiment. In this embodiment, the bonding wire 34 is extended between the bonding pad 32_{Y1} of the semiconductor chip 30 and the relay pad 32_{Y1}' of the semiconductor chip 26 and between the relay pad 32_{Y0}' and the connecting bonding pad 16_{Y0} of the circuit board 14, so that the bonding pad 32_{Y1} is electrically connected with the bonding pad 16_{Y0} which is shifted from the bonding pad 32_{Y1} in the Y-Y' direction without any possibility of the interference of the bonding wires. Also, this embodiment only requires the relay pad or bonding pads on the second semiconductor chip 26. Further, no change is needed for the mask pattern of the circuit board 14 or the second semiconductor chip 30. Furthermore, no bonding wire is required between the relay pads 16_{Y1}' and 32_{Y1}', which renders the wire bonding more simple and then inexpensive than that in the second embodiment. Besides, the total length of the bonding wire can be reduced. This in turn reduces an electric resistance in the circuit which would otherwise cause a

signal delay to increase the rise and fall times of signals.

FIFTH EMBODIMENT

Fig. 5 illustrates a part of the semiconductor device, generally indicated by reference numeral 10_4, according to the fifth embodiment of the present invention. In the semiconductor device 10_4, one bonding pad mounted on the semiconductor chip 30 beside its edge extending in the Y-Y' direction is electrically connected with another bonding pad mounted on the circuit board 14 beside its edge extending in the X-X' direction.

Specifically, a relay pad 32_{Y1}' is formed on a portion of the top surface of the semiconductor chip 26, beside its edge 38 extending in the Y-Y' direction, corresponding to the bonding pad 32_{Y1} formed on the top surface of the semiconductor chip 30, beside its edge 40 extending in the same direction. Also, a relay pad 32_{X0}' is formed on the top surface of the semiconductor chip 26, beside its edge 42 extending in the X-X' direction, corresponding to the bonding pad 16_{X0} formed on the circuit board 14, beside its edge 44 extending in the same direction. The relay pads 32_{Y1}' and 32_{X0}' are electrically connected with each other through a connecting wire or line 46 formed therein or thereon in the manufacturing process of the semiconductor chip 26. The circuit board 14 has a

solder ball (not shown) secured on its bottom surface and electrically connected with the bonding pad 16_{X0} by a through-hole (not shown). The bonding wires 34 are extended between the bonding pad 32_{Y1} and the relay pad $32_{Y1}'$ and between the relay pad $32_{X0}'$ and the connection pad 16_{X0}, which causes the bonding pad 32_{Y1} to be electrically connected with the bonding pad 16_{X0} which is shifted both in the X-X' and Y-Y' directions.

With the semiconductor device 10_4, each pad can electrically be connected with another pad which is shifted in the X-X' and Y-Y' directions beyond a range in which a wire bonding can be applied. Therefore, each connecting portion of the semiconductor device can be connected around to any portions of the mother board.

Although in this embodiment the connection pad positioned beside one edge of the semiconductor chip is connected with another connection pad positioned beside another neighboring edge of the circuit board, it may be connected with another connection pad positioned on the opposite side of the board since the circuit can be wired freely in the circuit board in the manufacturing process of the semiconductor device.

FIFTH EMBODIMENT

Fig. 6 illustrates a part of the semiconductor

device, generally indicated by reference numeral 10_5, according to the fifth embodiment of the present invention, which is a modification of the first embodiment. In the semiconductor device 10_5, the relay pad 16_{Y1}' formed on the circuit board 14 is electrically connected with the connecting bonding pad 16_{Y0} through the bonding wire 34. With the semiconductor device 10_5, similar to the first embodiment, the bonding pad 32_{Y1} can be connected with another bonding pad on the circuit board which is shifted from the bonding pad 32_{Y1} not only in the Y-Y' direction but also, by using another relay pad, in the X-X' direction.

SIXTH EMBODIMENT

Fig. 7 illustrates a part of the semiconductor device, generally indicated by reference numeral 10_6, according to the sixth embodiment of the present invention, which is a modification of the second embodiment. In the semiconductor device 106, a relay pad 32_{Y0}' is formed on the semiconductor chip 26. Also, the bonding wires 34 are extended between the bonding pad 32_{Y1} of the semiconductor chip 30 and the relay pad 16_{Y1}' of the circuit board 14, between the relay pad 16_{Y1}' on the circuit board 14 and the relay pad 32_{Y0}' on the semiconductor chip 26, and between the relay pad 32_{Y0}' of the semiconductor chip 26 and the connecting bonding pad 16_{Y0} on the circuit board 14. This

causes the bonding pad 32_{Y1} on the semiconductor chip 30 to be connected with another bonding pad 16_{Y0} on the circuit board which is shifted from the bonding pad 32_{Y1} in the Y-Y' direction.

With the semiconductor device 10_6, the bonding pad 32_{Y1} on the semiconductor chip 30 can be connected with another bonding pad on the circuit board 14 which is shifted spaced away from the bonding pad 32_{Y1} without any need to change the mask pattern of the semiconductor chip 30 and also without any interference of the bonding wires.

SEVENTH EMBODIMENT

Fig. 8 illustrates a part of the semiconductor device, generally indicated by reference numeral 10_7, according to the seventh embodiment of the present invention. In this semiconductor device 10_7, a connection pad 52_{Y1} of the semiconductor chip 30, which would be connected to a connection pad 50_{Y0} on the top surface of the circuit board, is formed on the bottom surface of the semiconductor chip 30. Also, a top surface 56 of the semiconductor chip 26 supporting the semiconductor chip 30 has a wire portion 58 formed on the surface 56 so that, when the semiconductor chip 30 is placed on the semiconductor chip 26, the connection pad 52_{Y1} faces to the wire portion 58. The wire portion 58 is extended outwardly

in the X-X' direction and then connected with another wire portion 60 formed in a marginal region surrounding around a region where the semiconductor chip 30 would occupy. The wire portion 60 is in turn connected through another wire portion 62 extending from the wire portion 60 in the X direction with a relay pad 64 also formed on the marginal region. The connection pad 52_{Y1} on the semiconductor chip 30 is connected with the wire portion 58 by placing the semiconductor chip 30 onto the semiconductor chip 26 and, at that moment, by holding a solder 66 between the connection pad 42_{Y1} and the wire portion 58. The solder 66 is heated to melt in a subsequent process, which causes the semiconductor chip 30 to make a close contact with the semiconductor chip 26. Then, the wire portion 64 of the semiconductor chip 26 is electrically connected with the connection pad 50_{Y0} of the circuit board 14 through the bonding wire 34.

With the semiconductor device 10_7, the connection pad on the semiconductor chip, even though it is formed on the surface confronting to the opposed semiconductor chip, can be wired to any connecting portion on the circuit board which is shifted from the connection pad in the X-X' and Y-Y' directions without causing the interference of the bonding wires. Also, even when the upper semiconductor chip 30 covers most of the opposing upper surface of the

lower semiconductor chip 26, the wire can be extended in the X-X' and/or Y-Y' direction within the limited marginal region in the top surface of the lower semiconductor. Further, the length of the bonding wire can be reduced, which in turn reduces time and cost for the wire bonding.

Although Fig. 8 shows one connection pad on the bottom surface of the semiconductor chip 30, more connection pad or all the pat electrode may be arranged on the bottom surface of the semiconductor chip 30. In the latter instance, no connection pad exists on the top surface of the semiconductor chip 30. This allows the connection pads to be connected with another connecting portions without using wire bonding and, thereby, reduces a height and then the size of the semiconductor device.

Of course, only a part of the number of electrodes, including the connection pad 52_{Y1}, may be formed on the bottom surface of the semiconductor chip with the remaining part of the connection pads positioned on the top surface of the semiconductor chip.

Also, although the solder is used for the connection of the opposing electrodes on the semiconductor chips 26 and 30, it may be replaced by another connecting technique.

EIGHTH EMBODIMENT

Fig. 9 illustrates a part of the semiconductor device, generally indicated by reference numeral 10_8, according to the eighth embodiment of the present invention, which is a modification of the seventh embodiment and is removed of wire portions 62 and 64 in the seventh embodiment shown in Fig. 8. Also, the circuit board 14 has connection pads 70_{Y0} and $70_{Y1}'$ formed thereon and spaced apart in the Y-Y' direction and a connection pad 72 connecting between the connection pads 70_{Y0} and $70_{Y1}'$. Further, the wire portion 60 and the connection pad $70_{Y1}'$ are electrically connected to each other by the bonding wire 68. With the semiconductor device 10_8, the same advantages can be attained as the seventh embodiment.

NINTH EMBODIMENT

Fig. 10 illustrates a part of the semiconductor device, generally indicated by reference numeral 10_9, according to the ninth embodiment of the present invention, which is a modification of the eighth embodiment. In this semiconductor device 109, the connection pad 70_{Y0} and the relay pad $70_{Y1}'$ are electrically connected by the bonding wire 34. With the semiconductor device 10_9, the same advantages can be attained as the seventh embodiment.

OTHER MODIFICATIONS

Although in the previous embodiments the circuit board is made of rectangular plate, it may be a lead frame which is made of conductive plate and then formed into a certain configuration.

Also, although in the previous embodiments the circuit board supports the first and second semiconductor chips, the present invention is not limited by the number of the semiconductor chips mounted on the circuit board.

ADVANTAGES OF THE INVENTION

As can be seen from above, according to the present invention the connection pads of the semiconductor chip can be connected with any connecting portions provided on the substrate without any restriction imposed by the wire bonding and beyond the wiring capability of the wire bonding.

Also, the semiconductor device according to the present invention can be mounted on a variety of mother boards without any need to change its circuit.

Further, the semiconductor device according to the present invention allows the semiconductor chip to be connected with the circuit board beyond the range in which the wire bonding can apply.

WHAT IS CLAIMED IS:

1. A semiconductor device mounted on a mother board, comprising:

a circuit board to be positioned on said mother board; and

a semiconductor chip positioned on said circuit board; wherein

(a) said circuit board has a connection pad, a relay pad spaced away from said connection pad, and a wire connecting between said connection pad and said relay pad on a surface of said circuit board supporting said semiconductor chip;

(b) said semiconductor chip has a connection pad corresponding to said connection pad formed on said circuit board; and

(c) said connection pad on said circuit board and said connection pad on said semiconductor chip are electrically connected through a bonding wire.

2. A semiconductor device in accordance with claim 1, wherein said wire connecting between said connection pad and said relay pad on said circuit board is printed on said circuit board with said connection pad and said relay pad.

3. A semiconductor device in accordance with claim 1,

wherein said wire connecting between said connection pad and said relay pad on said circuit board is a bonding wire.

4. A semiconductor device, comprising:

a first semiconductor chip having a connection pad;

a second semiconductor chip positioned on said first semiconductor chip, said second semiconductor chip having a connection pad, wherein said electrode on said second semiconductor chip is electrically connected with said connection pad on said first semiconductor chip.

5. A semiconductor device in accordance with claim 5, wherein said connection pad on said first semiconductor chip is connected with said connection pad on said second semiconductor chip through a bonding wire.

6. A semiconductor device in accordance with claim 5, wherein said connection pad on said first semiconductor chip positions in a region where said first semiconductor faces to said second semiconductor chip, said connection pad on said second semiconductor chip in said region, and said connection pad on said first semiconductor chip is electrically connected with said connection pad on said second semiconductor chip through a conductive member

positioned in said region.

7. A wiring method, comprising the steps of:

providing a first semiconductor chip having a connection pad;

positioning a second semiconductor chip on said first semiconductor chip, said second semiconductor chip having a connection pad; and

electrically connecting between said connection pad of said first semiconductor chip and said connection pad of said second semiconductor chip.

8. A wiring method in accordance with claim 8, wherein said connection pad of said first semiconductor chip is electrically connected with said connection pad of said second electrode through a bonding wire.

9. A wiring method in accordance with claim 8, wherein said connection pad on said first semiconductor chip positions in a region where said first semiconductor faces to said second semiconductor chip, said connection pad on said second semiconductor chip positions in said region, and said connection pad on said first semiconductor chip is electrically connected with said connection pad on said second semiconductor chip through a conductive member

positioned in said region.

ABSTRACT OF THE DISCLOSURE

A semiconductor device mounted on a mother board has a circuit board to be positioned on the mother board and a semiconductor chip positioned on the circuit board. The circuit board has a connection pad, a relay pad spaced away from the connection pad, and a wire connecting between the connection pad and the relay pad on a surface of the circuit board supporting the semiconductor chip. Also, the semiconductor chip has a connection pad corresponding to the connection pad formed on the circuit board. Further, the connection pad on the circuit board and the connection pad on the semiconductor chip are electrically connected to each other through a bonding wire.

Fig.1

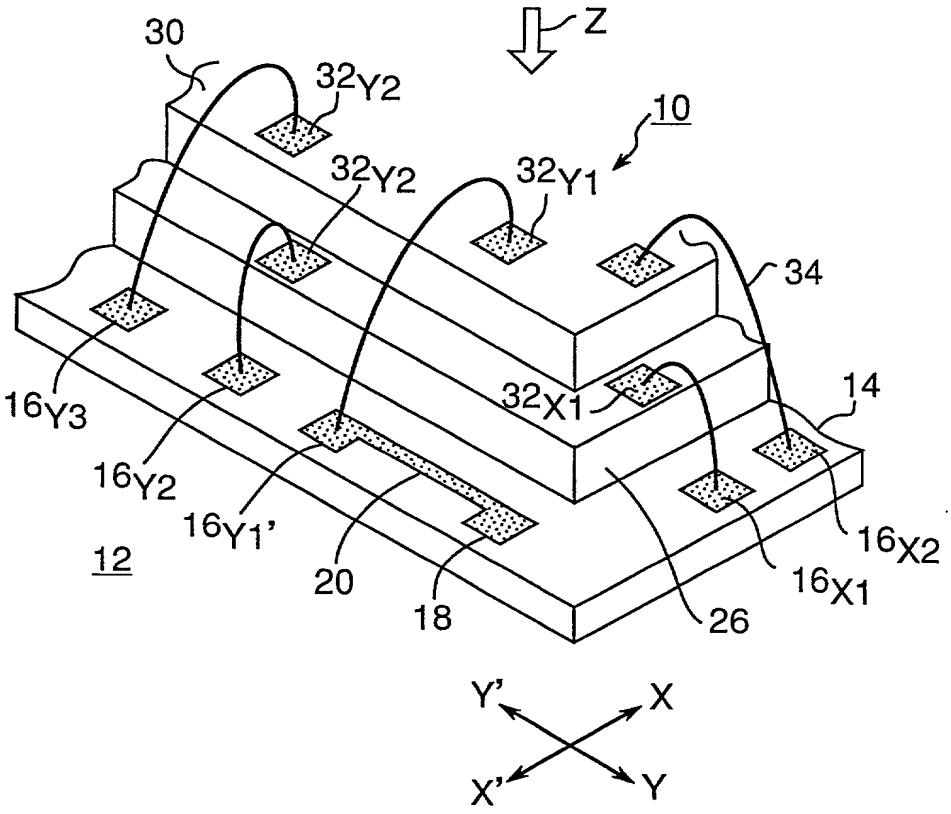

30
Z
32Y2
10
32Y2
32Y1
34
16Y3
32X1
14
16Y2
16Y1'
12
20
18
26
16X1
16X2
Y'
X
X'
Y

Fig.2

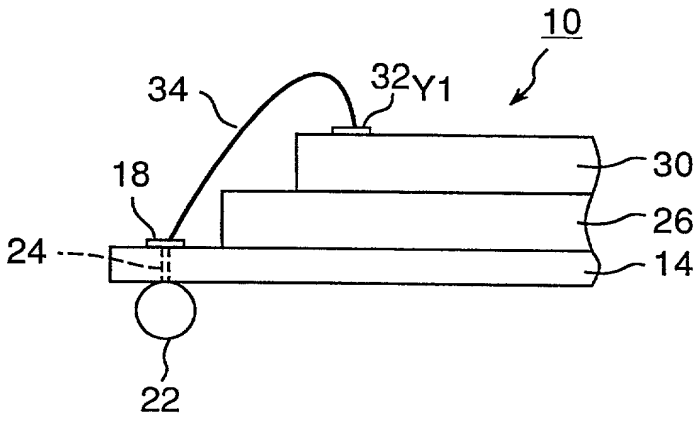


Fig.3

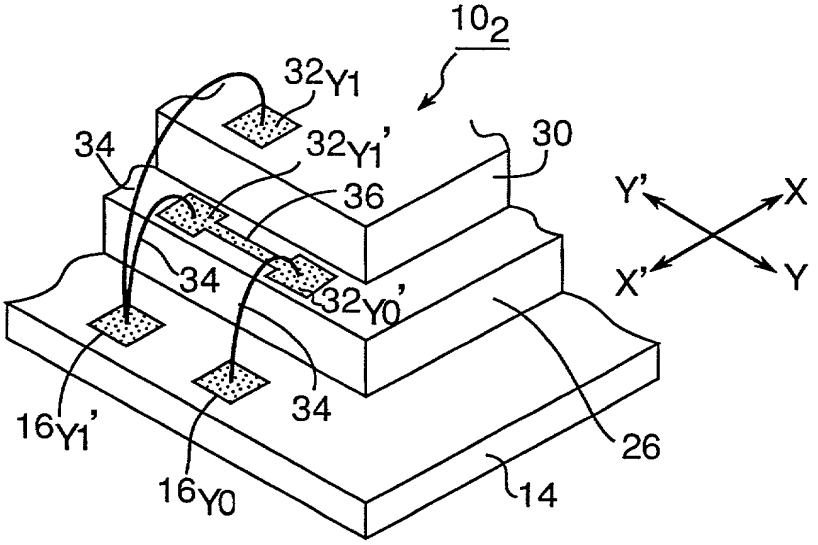

10_2
32_{Y1}
$32_{Y1}'$
34
30
36
Y'
X
X'
Y
34
$32_{Y0}'$
$16_{Y1}'$
34
26
16_{Y0}
14

Fig.4

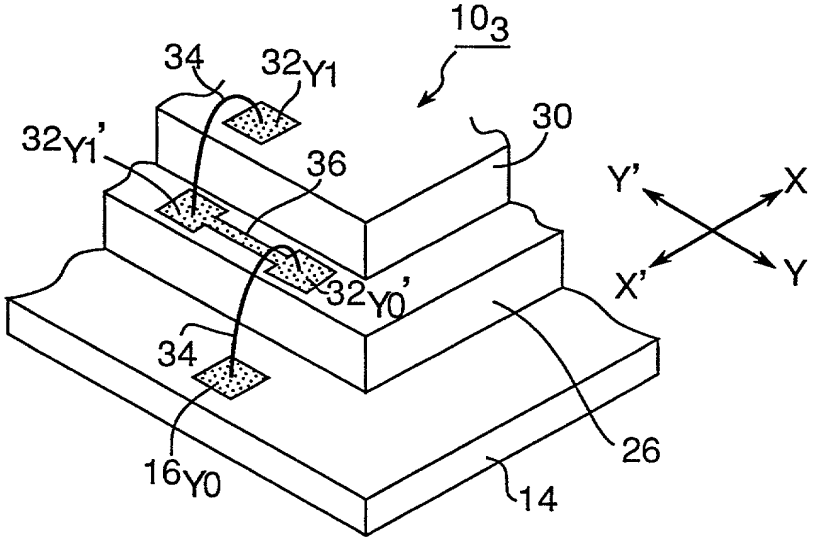

10_3
34
32_{Y1}
$32_{Y1}'$
30
36
Y'
X
X'
Y
$32_{Y0}'$
34
26
16_{Y0}
14

Fig.5

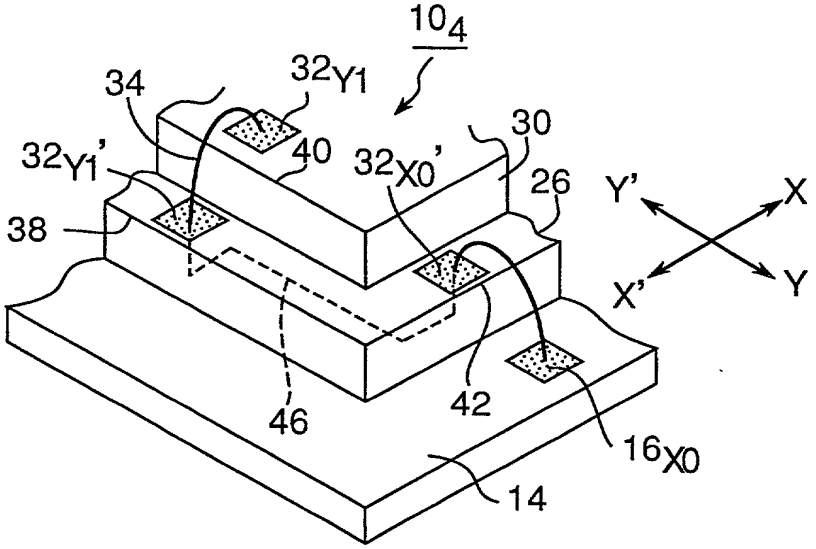

10_4
32_{Y1}
34
30
$32_{Y1}'$
40
$32_{X0}'$
26
Y'
X
38
X'
Y
46
42
16_{X0}
14

Fig.6

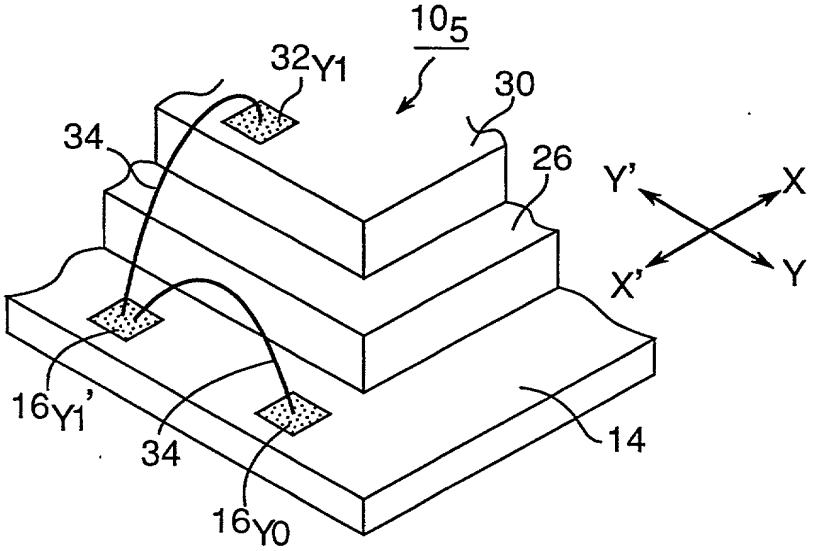

10_5
32_{Y1}
30
34
26
Y'
X
X'
Y
$16_{Y1}'$
34
14
16_{Y0}

Fig.7

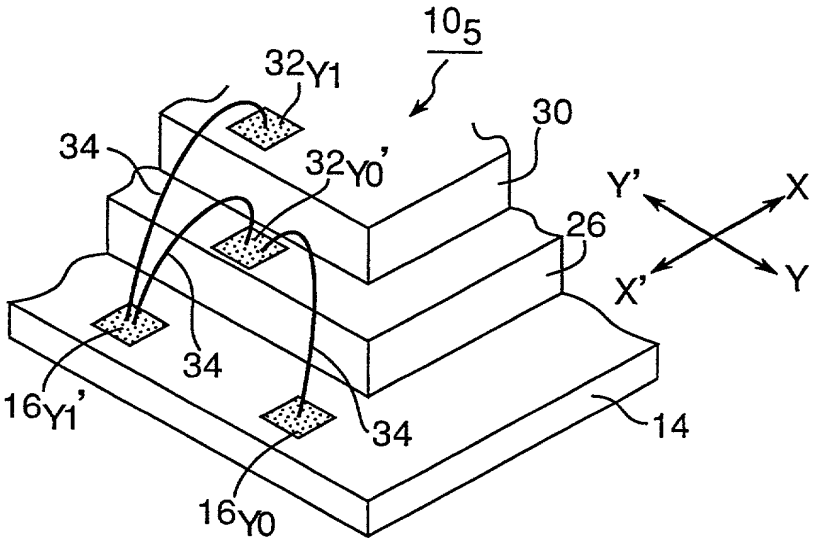


Fig.8

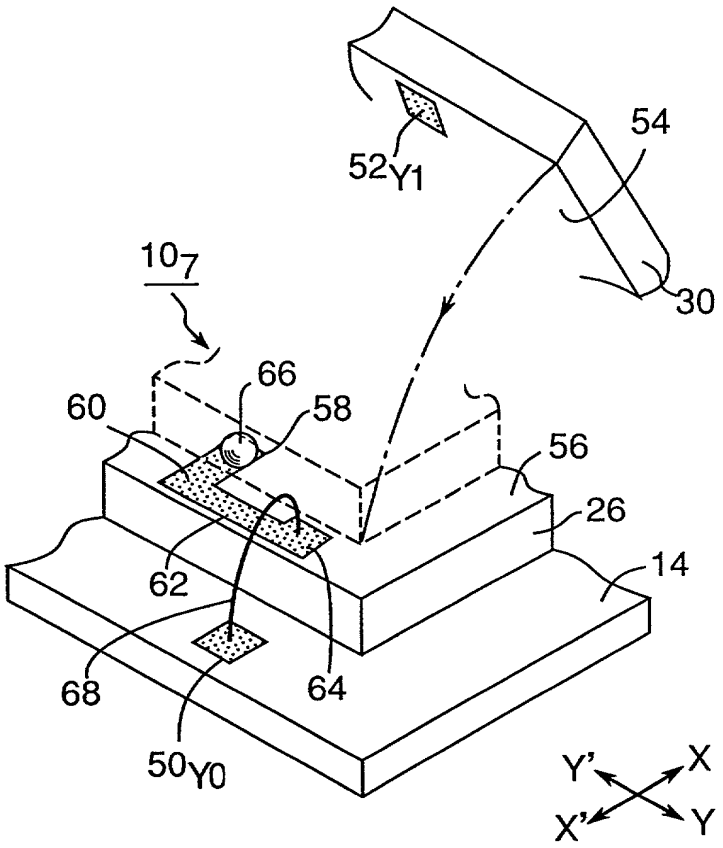


Fig.9

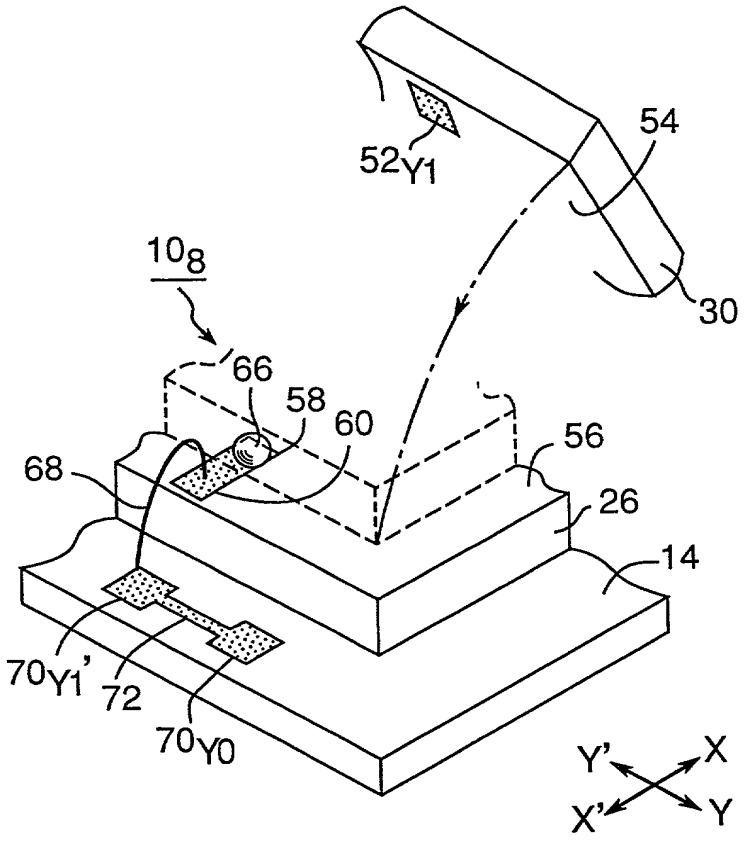


Fig.10

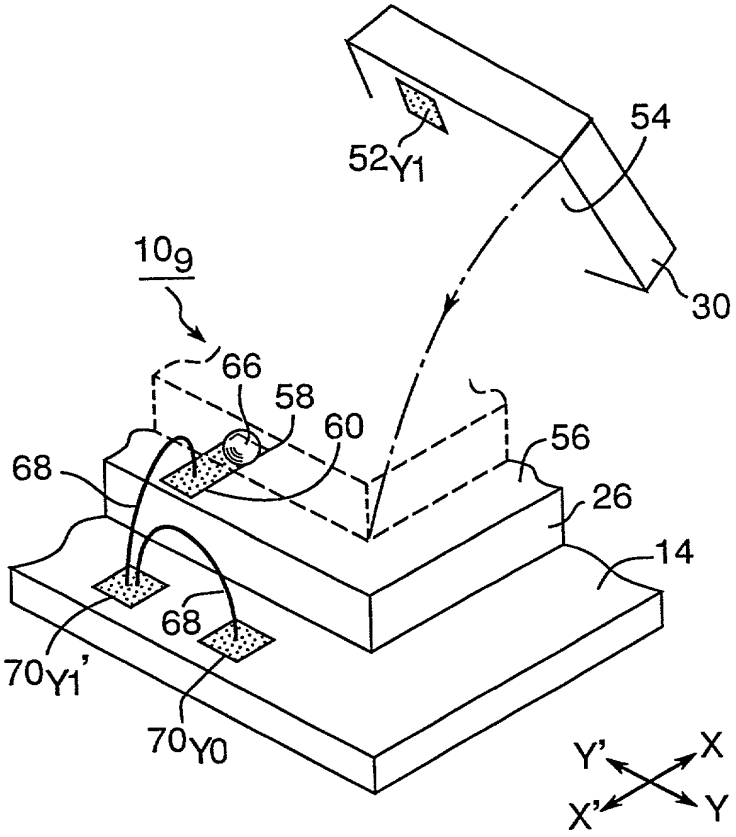


Fig.11 PRIOR ART

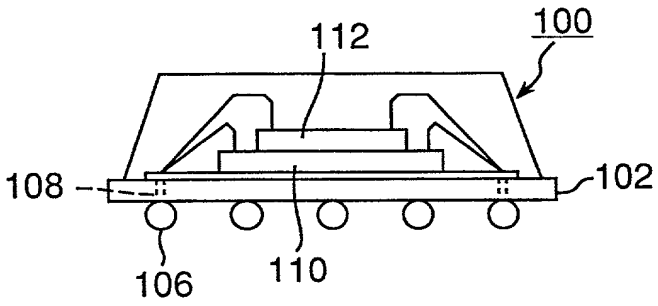
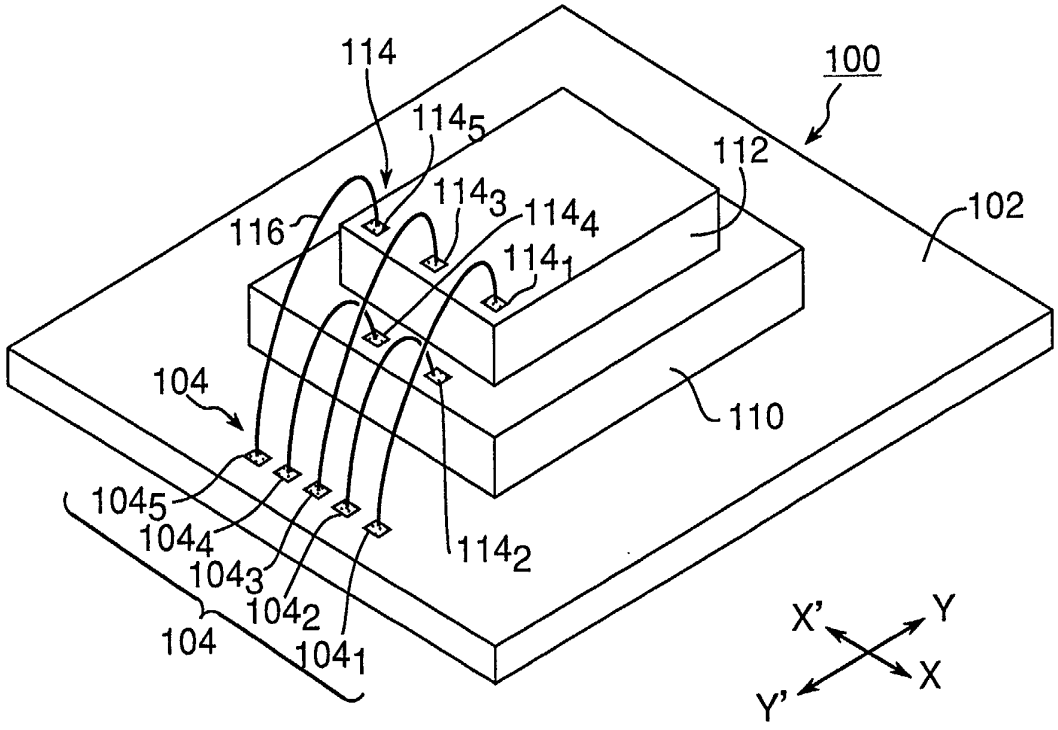


Fig.12 PRIOR ART



Declaration and Power of Attorney for Patent Application
特許出願宣告書

Japanese Language Declaration

私は、下欄に氏名を記載した発明者として、以下のとおり宣言する。：	As a below named inventor, I hereby declare that:
私の住所、郵便の宛先および国籍は、下欄に氏名に続いて記載したとおりであり、	My residence, post office address and citizenship are as stated below next to my name,
名称の発明に関し、請求の範囲に記載した特許を求める主題の本来の、最初にして唯一発明者である（一人の氏名のみが下欄に記載されている場合）か、もしくは本来の最初にして共同の発明者である（複数の氏名が下欄に記載されている場合）と信じ、	I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled.
_____	SEMICONDUCTOR DEVICE AND ITS WIRING
_____	METHOD
_____	_____
その明細書を （該当する方に印を付す） ☐ ここに添付する。	the specification of which (check one) ☒ is attached hereto.
☐ _____日に出願番号	☐ was filed on_____as
第_____号として提出し、	Application Serial No. _____
_____日に補正した。 （該当する場合）	and was amended on _____. (if applicable)
私は、前記のとおり補正した請求の範囲を含む前記明細書の内容を検討し、理解したことを陳述する。	I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment refereed to above.
私は、連邦規則法典第 37 部第 1 章第 56 条(a)項に従い、本願の審査に所要の情報を開示すべき義務を有することを認める。	I acknowledge the duty to disclose information which is material to the examination of this application in accordance with the Title 37, Code of Federal Regulations, § 1.56(a).

Japanese Language Declaration

私は、合衆国法典第 35 部第 119 条にもとづく下記の外国特許出願または発明者証出願の外国優先権利益を主張し、さらに優先権の主張に係わる基礎出願の出願日前の出願日を有する外国特許出願または発明者証出願を以下に明記する：

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)
先の外国出願

(Number) (番 号)	(Country) (国 名)	(Day/Month/Year Filed) (出願の年月日)	Priority Claimed 優先権の主張
2000-7923	Japan	17/January/2000	☒ Yes あり ☐ No なし
			☐ Yes あり ☐ No なし
			☐ Yes あり ☐ No なし

私は、合衆国法典第 35 部第 120 条にもとづく下記の合衆国特許出願の利益を主張し、本願の請求の範囲各項に記載の主題が合衆国法典第 35 部 112 条第 1 項に規定の態様で先の合衆国出願に開示されていない限度において、先の出願の出願日と本願の国内出願日または PCT 国際出願日の間に公表された連邦規則法典第 37 部第 1 章第 56 条(a)項に記載の所要の情報を開示すべき義務を有することを認める：

I hereby claim the benefit under Title 35, United States Code, § 120 of any United Sates application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56 (a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.) (出願番号)	(Filing Date) (出願日)	(Status:patented, pending, abandoned) (現況:特許済、係属中、放棄済)

私は、ここに自己の知識にもとづいて行った陳述がすべて真実であり、自己の有する情報および信ずるところに従って行った陳述が真実であると信じ、さらに故意に虚偽の陳述等を行った場合、合衆国法典第 18 部第 1001 条により、罰金もしくは禁錮に処せられるか、またはこれらの刑が併科され、またかかる故意による虚偽の陳述が本願ないし本願に対して付与される特許の有効性を損うことがあることを認識して、以上の陳述を行ったことを宣言する。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration

委任状：私は、下記発明者として、以下の代理人をここに選任し、本願の手続を遂行すること並びにこれに関する一切の行為を特許商標庁に対して行うことを委任する。（代理人氏名および登録番号を明記のこと）

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

Stanislaus Aksman, Reg. No. 28,562; Edward A. Becker, Reg. No. 37,777; Stephen A. Becker, Reg. No. 26,527; William H. Beha, Reg. No. 38,038; John G. Bisbikis, Reg. No. 37,095; Kenneth L. Cage, Reg. No. 26,151; Stephen C. Carlson, Reg. No. 39,929; Paul Devinsky, Reg. No. 28,553; Laura A. Donnelly, Reg. No. 38,435; Margaret M. Duncan, Reg. No. 30,879; Brian E. Ferguson, Reg. No. 36,801; Michael F. Fogarty, Reg. No. 36,139; Wilhelm F. Gadiano, Reg. No. 37,136; Keith E. George, Reg. No. 34,111; John A. Hankins, Reg. No. 32,029; Thomas A. Jolly, Reg. No. 39,241; Eric J. Kraus, Reg. No. 36,190; Edward E. Kubasiewicz, Reg. No. 30,020; Robert E. LeBlanc, Reg. No. 17,219; Jack Q. Lever, Reg. No. 28,149; Raphael V. Lupo, Reg. No. 28,363; Christine F. Martin, Reg. No. 39.762; Michael E. McCabe, Jr., Reg. No. 37,182; James H. Meadows, Reg. No. 33,965; Michael A. Messina, Reg. No. 33,424; Joseph H. Paquin, Jr., Reg. No. 31,647; Craig L. Plastrik, Reg. No. 41,254; Robert L. Price, Reg. No. 22,685; Paul A. Roberts, Reg. No. 40,289; Gene Z. Rubinson, Reg. No. 33,351; Joy Ann G. Serauskas, Reg. No. 27,952; Michele M. Schafer, Reg. No. 34,717; David J. Serbin, Reg. No. 30,589; Glenn Snyder, Reg. No. 41,428; Arthur J. Steiner, Reg. No. 26,106; David L. Stewart, Reg. No. 37,578; Leonid D. Thenor, Reg. No. 39,397; Keith J. Townsend, Reg. No. 40,358; Leon R. Turkevich, Reg. No. 34,035; Christopher D. Ward, Reg. No. 41,367; Damian G. Wasserbauer, Reg. No. 34,749; Edward J. Wise, Reg. No. 34,523; Alexander V. Yampolsky, Reg. No. 36,324; and Robert W. Zelnick, Reg. No. 36,976

書類の送付先：

Send Correspondence to:
McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, D.C. 20005-3096

直接電話連絡先：（名称及び電話番号）

Direct Telephone Calls to: (name and telephone number)
Stephen A. Becker
(202) 756-8000

唯一のまたは第一の発明者の氏名	Full Name of First Joint Inventor Isao NOJIRI
同発明者の署名　　日付	First inventor's signature　　Date Isao Nojiri　　August 21, 2000
住所	Residence Tokyo, Japan
国籍	Citizenship Japan
郵便の宛先	Post Office Address c/o Mitsubishi Denki Kabushiki Kaisha, 2-3, Marunouchi 2-chome, Chiyoda-ku, TOKYO 100-8310 JAPAN
第二の共同発明者の氏名（該当する場合）	Full Name of Second Joint Inventor Ryu MAKABE
同第二発明者の署名　　日付	Second inventor's signature　　Date Ryu Makabe　　August 21, 2000
住所	Residence Tokyo, Japan
国籍	Citizenship Japan
郵便の宛先	Post Office Address c/o Mitsubishi Denki Kabushiki Kaisha, 2-3, Marunouchi 2-chome, Chiyoda-ku, TOKYO 100-8310 JAPAN

（第三またはそれ以降の共同発明者に対しても同様な情報および署名を提供すること。）

(Supply similar information and signature for third and subsequent joint inventors.)